TEMIC

Siliconix

AN103

The FET Constant-Current Source/Limiter

Introduction

The combination of low associated operating voltage and high output impedance makes the FET attractive as a constant-current source. An adjustable-current source (Figure 1) may be built with a FET, a variable resistor, and a small battery. For optimum thermal stability, the FET should be biased near the zero temperature coefficient point.

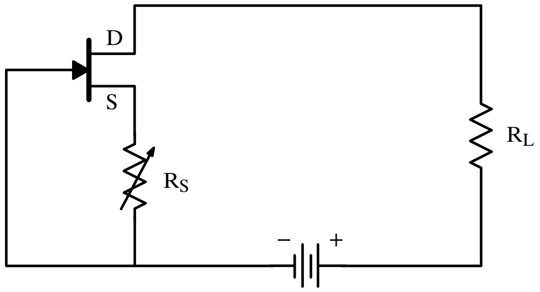


Figure 1. Field-Effect Transistor Current Source

Whenever the FET is operated in the current saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is at least 50% greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant-current source at any current below its saturation current I_{DSS}.

Basic Source Biasing

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)}\left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \qquad (1)$$

where k can vary from 1.8 to 2.0, depending on device geometry. If K = 2.0, the series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad \text{or} \quad R_S = \frac{V_{GS(off)}}{I_D}\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right) \qquad (2)$$

A change in supply voltage or a change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = (\Delta V_{DS})(g_{oss}) \qquad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant-current source where the supply voltage may vary. As g_{oss} may range from less than 1 µS to more than 50 µS according to the FET type, the dynamic impedance can be greater than 1 MΩ to less than 20 kΩ. This corresponds to a current stability range of 1 µA to 50 µA per volt. The value of g_{oss} also depends on the operating point. Output conductance g_{oss} decrease approximately linearly with I_D. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \qquad (4)$$

$$\text{where } g_{oss} = g'_{oss} \qquad (5)$$

$$\text{when } V_{GS} = 0 \qquad (6)$$

So as $V_{GS} \rightarrow V_{GS(off)}$, $g_{oss} \rightarrow$ Zero. For best regulation, I_D must be considerably less than I_{DSS}.

Cascading for Low g_{oss}

It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs, as shown in Figure 2.

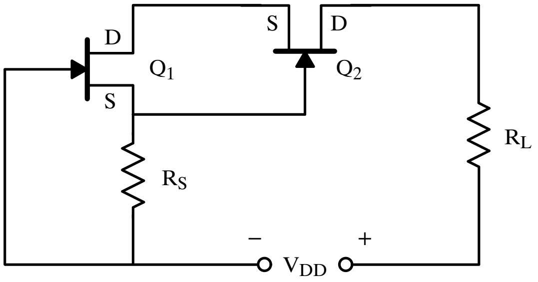
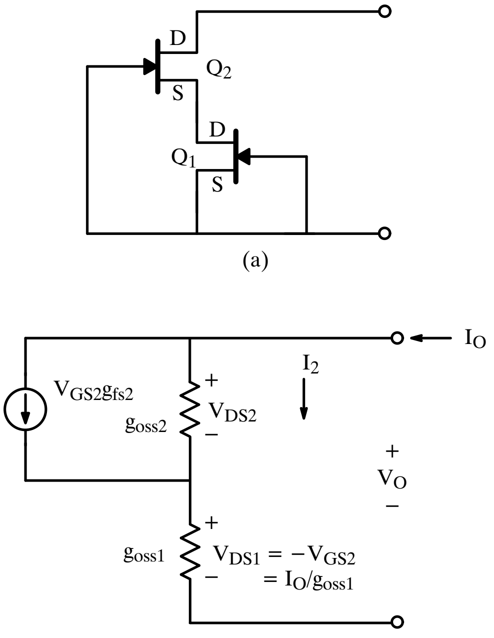


Figure 2. Cascade FET Current Source



(a)

(b)

Figure 3. Cascade FET $V_{GS1} = 0$

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The dc value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

If $g_{oss1} = g_{oss2}$ (7)

$$g_o = \frac{g_{oss}}{2 + \frac{g_{fs}}{g_{oss}}} \tag{8}$$

when RS ≠ 0 as in Figure 2

$$g_o \approx \frac{{g_{oss}}^2}{g_{fs}(1 + R_S g_{fs})} \tag{9}$$

In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably lower than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage, V_{DG}. That is,

$V_{DG} > V_{GS(off)}$, preferably $V_{DG} > 2V_{GS(off)}$ (10)

If $V_{DG} < 2\ V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A JFET may have a typical $g_{oss} = 4\ \mu S$ at $V_{DS} = 20$ V and $V_{GS} = 0$. At $V_{DS} \sim -V_{GS(off)} = 2$ V, $g_{oss} \sim 100\ \mu S$.

The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4340, J202, and SST202 exhibit typical $g_{oss} = 2\ \mu S$ at $V_{DS} = 20$ V. These devices in the circuit of Figure 4 will provide a current source adjustable from 5 μA to 0.8 mA with internal impedance greater than 2 MΩ at 0.2 mA. Other Siliconix part types such as the 2N4392, J112, and SST112 can provide 10 mA or higher current.

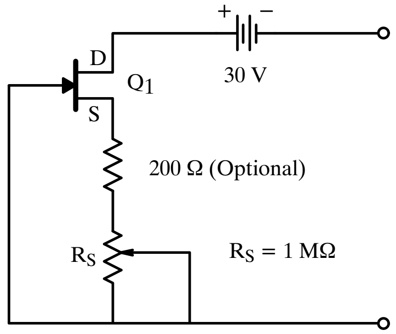


Figure 4. Adjustable Current Source $R_S = 1\ M\Omega$

Instead of the adjustable resistor, the JFETs can be put in I_{DSS} range groupings with an appropriate R_S resistor selected for each group. This method is common in high volume applications.

The cascade circuit of Figure 5 provides a current adjustable from 2 μA to 0.8 mA with internal resistance greater than 10 MΩ.

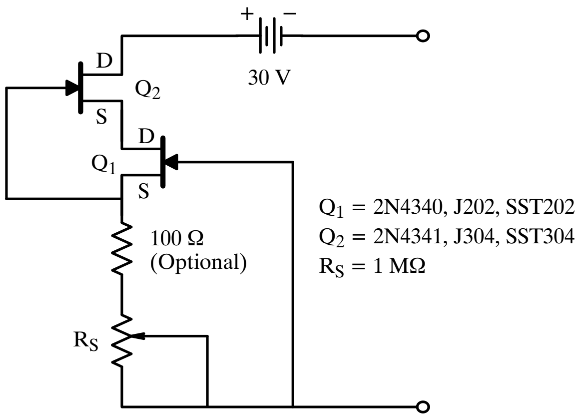


Figure 5. Cascade FET Current Source

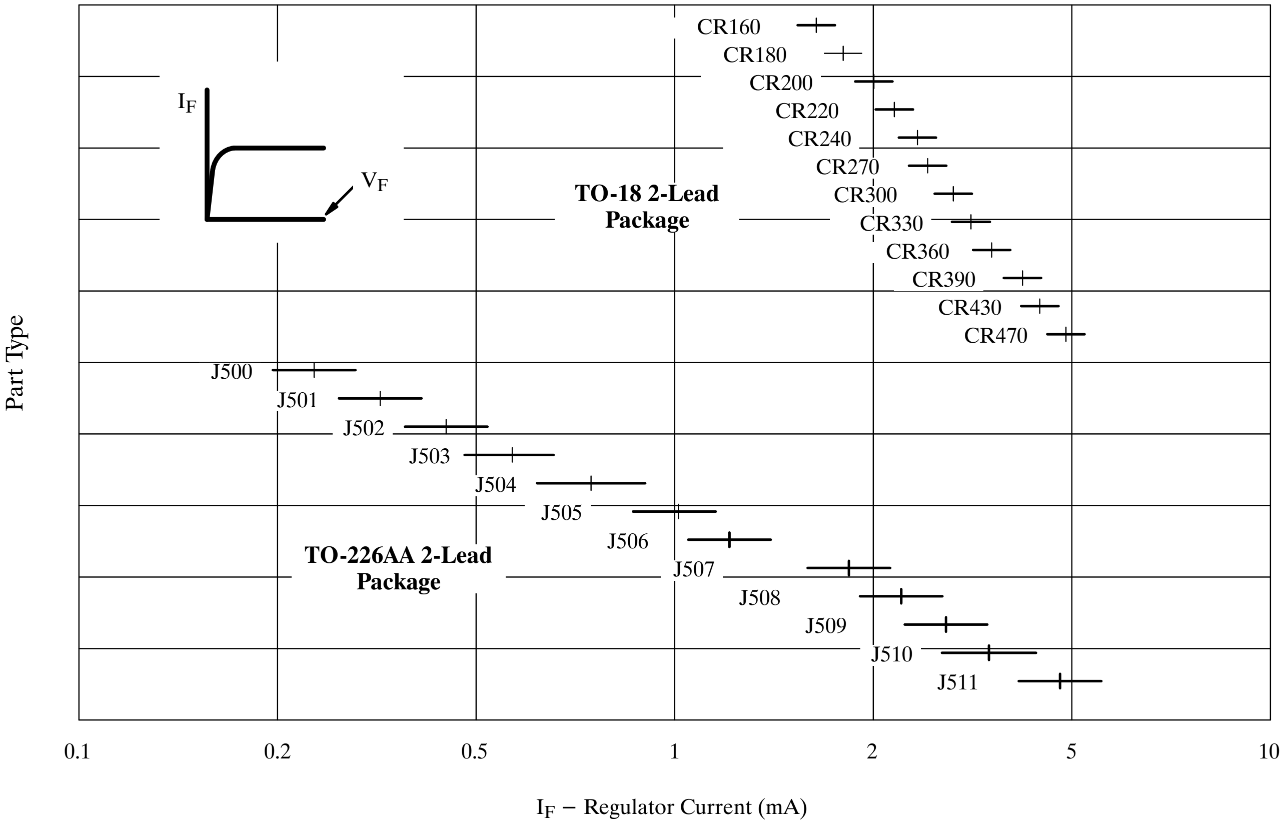


Figure 6. Standard Series Current Regulator Range

Standard Two-Leaded Devices

Siliconix offers a special series of two-leaded JFETs with a resistor fabricated on the device, thus creating a ± 10% current range. Devices are available in ranges from 1.6 mA (CR160) to 4.7 mA (CR470).

For designs requiring a ± 20% current range, Siliconix offers devices rated from 0.24 mA typical (J500) through 4.7 mA typical (J511) in a two-leaded TO-226A (TO-92) package.

Each of these two-leaded devices can be used to replace several typical components.

Figure 6 shows the current ranges of these two device series. Further information is contained in the individual data sheets appearing elsewhere in this data book or from Siliconix FaxBack.

The CR160 series features guaranteed peak operating voltage minimum of 100 V with a typical of 180 V. The J500 series features 50 V minimum with a typical of 100 V. The lower current devices in both series provide excellent current regulation down to as little as 1 V.

Bias Resistor Selection

All industry JFET part types exhibit a significant variation in I_{DSS} and $V_{GS(off)}$ on min/max specifications and device-to-device variations.

Using the simple source biasing current source as illustrated in Figure 1, the designer can graphically calculate the R_S which best fits the desired drain current I_D. Figure 7 plotting I_D versus V_{GS} over the military temperature range shows the resulting I_D for different values of R_S.

The R_S lines are constructed by drawing the slope of the R_S desired value starting at the origin, eg. R_S = 2 k slope. Find a convenient point on the X – Y axis to mark a $\frac{V_{GS}}{I_D}$ of 2 kΩ such as $V_{GS} = -1.5$ V and $I_D = 0.75$ mA.

Then, draw a straight line from this point to the origin. The intersection of this R_S line and the device I_D versus V_{GS} will be the operating I_D. In this example, the resulting $I_D = 0.35$ mA at $T_J = 25°C$. The intercepts of the $T_J = -55°C$ and 125°C show the minimal variation with temperature.

Also note that JFETs have a I_D current where there is no change with temperature variation. To achieve this $0T_C$, the $-V_{GS}$ voltage (I_D x R_S) is approximately:

$$V_{GS(0TC)} \simeq V_{GS(off)} - 0.65 \text{ V} \qquad (11)$$

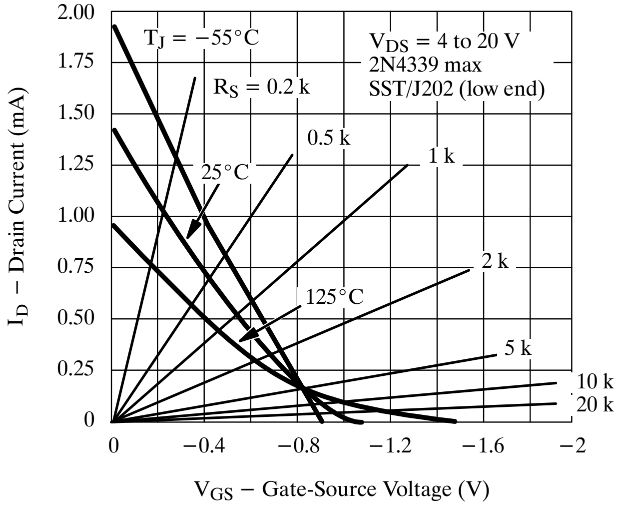


Figure 7. JFET Typical Transfer Characteristic

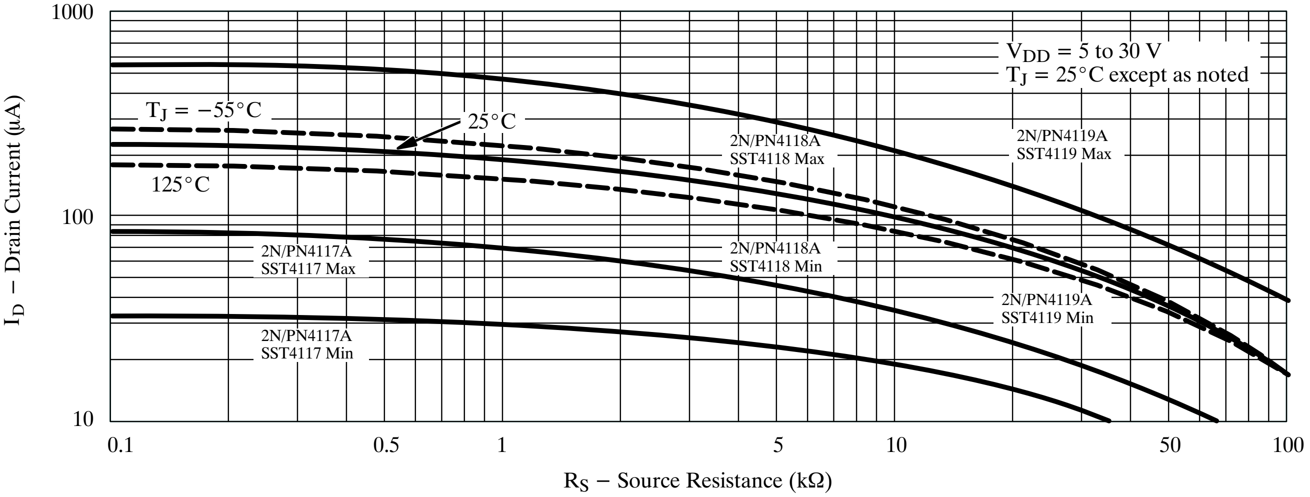


Figure 8. Source Biased Drain-Current vs. Source Resistance

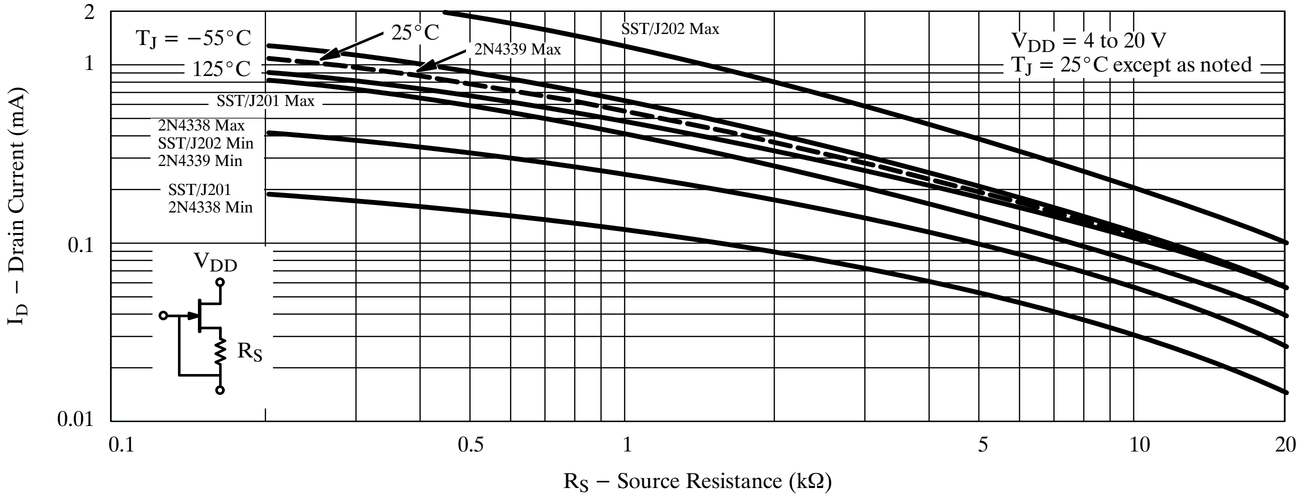


Figure 9. JFET Source Biased Drain-Current vs. Source Resistance

Choosing the Correct JFET for Source Biasing

Each of the Siliconix device data sheets include typical transfer curves that can be used as illustrated in Figure 7.

Several popular devices are ideal for source biased current sources covering a few μAs to 20 mA. To aid the designer, the devices in Table 1 have been plotted to show the drain current, I_D, versus the source resistance, R_S, in Figures 8, 9, and 10. Most plots include the likely worst case I_D variations for a particular R_S. For tighter current control, the JFET production lot can be divided into ranges with an appropriate resistor selection for each range.

Table 1: Source Biasing Device Recommendations

Practical Current Range I_D (mA)	**Through-Hole Plastic Device**	**Surface Mount Device**	**Metal Can Device**
0.01 − 0.02	PN4117A	SST4117	2N4117A
0.01 − 0.04	PN4118A	SST4118	2N4118A
0.02 − 0.1	PN4119A	SST4119	2N4119A
0.01 − 0.1	J201	SST201	2N4338
0.02 − 0.3	J202	SST202	2N4339
0.1 − 2	J113	SST113	2N4393
0.2 − 10	J112	SST112	2N4392

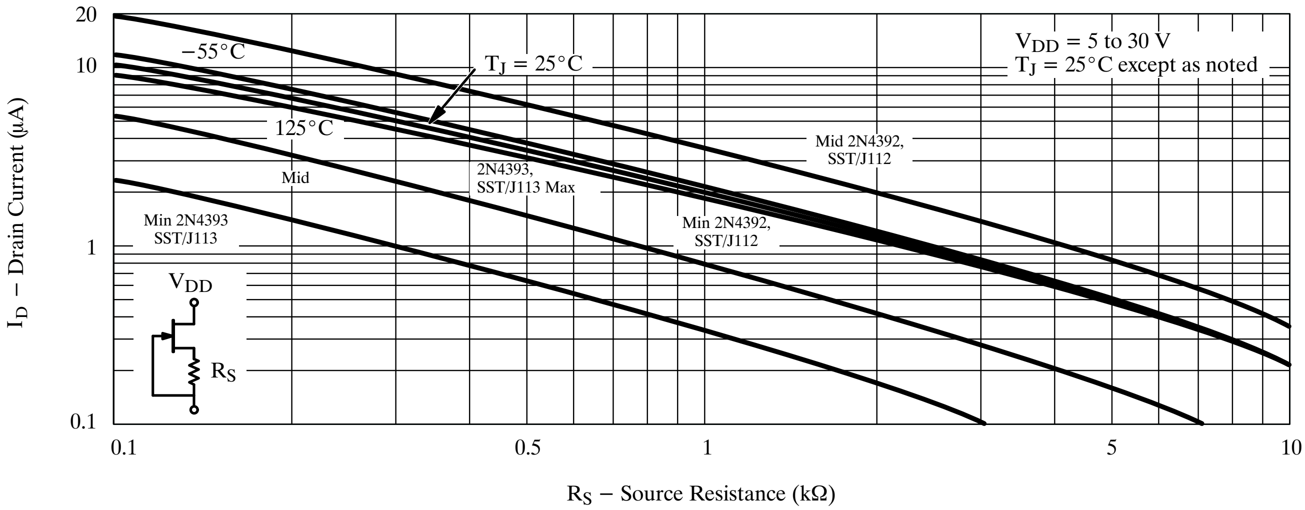


Figure 10. JFET Source Biased Drain-Current vs. Source Resistance